F I G. 1

F I G. 2

DELAY

DPSW1

TFG

31-1

Vin

31-2

TFG

Vout

/DPSW1

12

F I G . 3

DELAY

/DPSW1

P1

Idp1

N1

Idn1

31-1

DPSW1

Vin

Vout

DPSW1

31-2

P2

Idp2

N2

Idn2

/DPSW1

Idp1<Idp2, Idn1<Idn2

F I G . 4

DEC

51

/RD1 ———

⋮

RDn ———

——— DPSW1

13

F I G. 5

DEC

/RD1 ———
RD2 ———
RD3 ———
RD4 ———

51-1

——— DPSW1

RD1 ———
/RD2 ———
RD3 ———
RD4 ———

51-2

——— DPSW2

RD1 ———
RD2 ———
/RD3 ———
RD4 ———

51-3

——— DPSW3

RD1 ———
RD2 ———
RD3 ———
/RD4 ———

51-4

——— DPSW4

13

F I G. 6

F I G. 7

F I G. 8

DELAY

P1 /DPSW1 Idp1

R1 N1 Idn1

31-1 DPSW1

Vin Vout

DPSW1 31-2

P2 Idp2

R2 N2 Idn2

/DPSW1

R1 > R2, Idp1 ≦ Idp2, Idn1 ≦ Idn2

12'

F I G. 9

DEC

81-1

/RD1
RD2
⋮
RDn

81-2

81-3

RD1
/RD2
⋮
/RDn

DPSW1

13'

F I G. 10

F I G. 11A

13"

91U

RDU (1)

DPDEC0U

DPDEC1U

(2)

DPDEC0L

DPDEC1L

91L

1) Decode with a half of the data (Miniaturization of decode circuit)

[00000001 00001111]
(1)   (2)

F I G. 11B

13"

All bit "0"
92UU (3)—DPALLUU0
92UL (4)—DPALLUL0
92LU (5)—DPALLLU0
92LL (6)—DPALLLL0

All bit "1"
93UU (3)—DPALLUU1
93UL (4)—DPALLUL1
93LU (5)—DPALLLU1
93LL (6)—DPALLLL1

2) Confirm data coincidence by dividing data into quarter

[0000 0001 0000 1111]
(3) (4) (5) (6)

F I G. 11C

13"

DPALLLU0
DPALLLL0
DPDEC0U

DPALLLU1
DPALLLL1
DPDEC1U

DPSWU

DPALLUU0
DPALLUL0
DPDEC0L

DPALLUU1
DPALLUL1
DPDEC1L

DPSWL

F I G. 12

DELAY

D1 ○—————•——[FIFO]————————————————————[⟋⟋]———————▷○

DPSW12

17-12

18-1

D2 ○—————•——[FIFO]————————————————————[⟋⟋]———————▷○

DPSW23

17-23

18-2

D3 ○—————•——[FIFO]————————————————————[⟋⟋]———————▷○

18-3

F I G. 13

RDn ————▷ [FIFO] ——QRn——▷ [OCD] ————▷ DQn

101   102

↑
OUTCLK

F I G. 14 PRIOR ART

F I G. 15A PRIOR ART

Ca>Cb, Ra>Rb, Za>Zb

F I G. 15B PRIOR ART

Wiring 2   Wiring 1   Wiring 3
Point A

F I G. 16A
PRIOR ART

Point B

C12   C13

F I G. 16B
PRIOR ART

| Wiring 2 |—| |—| Wiring 1 |—| |—| Wiring 3 |
C1

	Wiring 2	Wiring 1	Wiring 3	Data pattern
Potential change	↗	↗	↗	In-phase
	↘	↗	↘	Reverse phase
	↘	↘	↘	In-phase
	↗	↘	↗	Reverse phase

F I G. 16C
PRIOR ART

Voltage

Point A

1/2Volt

Point B
(reverse phase)

Point B
(In-phase)

Time

F I G. 16D
PRIOR ART

Potential change (△V) by the transient current which flows the power source GND

$$\triangle V = N \cdot L_{eff} \cdot (di/dt)$$

Effective inductance (Leff) of PKG (power source)

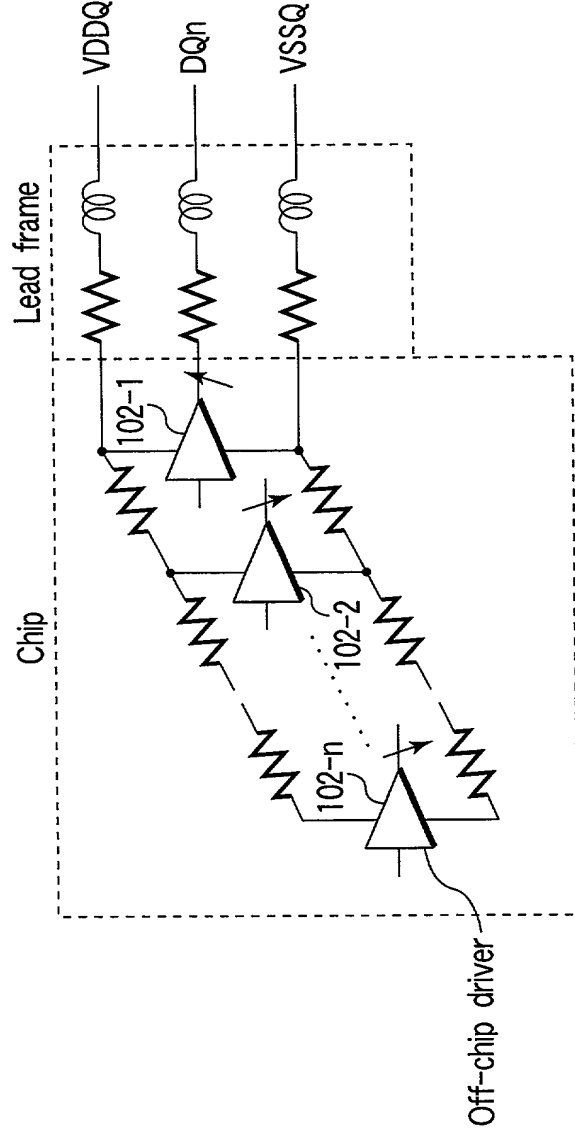Current drive performance (di/dt) of the driver

Simultaneous switching number (N)

Lead frame

VDDQ

DQn

VSSQ

Chip

102-1

102-2

102-n

Off-chip driver

FIG.17 PRIOR ART

Access time

I

II

All HIGH→LOW

One bit reverse phase

Two bit reverse phase

Data pattern

Two bit reverse phase

One bit reverse phase

All LOW→HIGH

F I G. 18 PRIOR ART